AMENDMENTS TO SPECIFICATION

Please amend the following paragraph in the specification as indicated.

[0021] The operation of the computer system 100 will now be described with reference to FIG. 2. In order to boot the slave processing units 112 and 122 from the volatile memory devices 114 and 124, respectively, the programmable logic device 108 contains logic to correctly combine the second processing unit's memory interface signals and the hardware handshake signals of the ~~volatile memory device 114, 124~~ master processor 102 to `trick` the slave processing units 112, 122 into thinking that they are being bootstrapped using flash devices. First, the first processing unit 102 is bootstrapped in a known manner using the flash device 106. During system initialization 202 (and board reset release), the first processing unit commands the programmable logic device to generate and assert the reset lines 118, 128 of the slave processing units in step 204. The reset lines to all processors are asserted 204 after power up 202 automatically from the CPLD. Then, after a preset time, the first processor's reset line is automatically brought out of reset 206, from which it continues its bootstrapping sequence 208. The first processor can re-reset and restart 210 the bootstrapping sequence to the second, third, etc . . . processors, if for any reasons a processor fault occurs during execution or a newer bootstrap code is needed to replace the current code in the volatile memory. This can occur not only at power up. The first processing unit then commands the programmable logic device to generate and assert the reset lines 118, 128 of the slave processing units in step 212. The first processing unit 102 then loads the boot code for the slave processing units 112, 122 from the flash device to the volatile memory devices 114, 124 using the local bus 110 in step 214. The first processing unit 102 then commands the programmable logic device 108 to de-assert the reset lines 118, 128 of the second processing units 112, 122 in step 216. The second processing units 112, 122 then accept the boot code from the volatile memory device 114, 124, respectively, and perform their bootstrap procedure in step 218. This is followed by loading of application and starting of application code in step 220. This code can be loaded through shared volatile memory or through other communication mechanisms e.g. PCI as described.